

BM60052FV-C Evaluation Board (For 300 A/1200 V Full-SiC Power Module Drive)

BM60052FV-EVK-001

1-1. Overview

BM60052FV-EVK-001 (BM60052FV-C Evaluation Board) is an evaluation board whose shape allows direct mounting onto the ROHM's 2ch 300 A/1200 V class full-SiC power module, BSM300D12P2E001.

This is a single unit, comprising the SiC-MOSFET gate drive circuit along with the gate driver IC, the BM60052FV-C integrating insulation element, and an insulated DC-DC converter, supplying gate voltage.

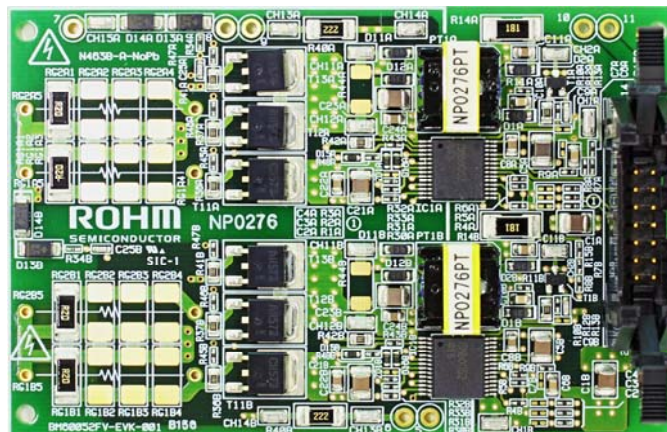
The constant is set to the value suitable for driving BSM300D12P2E001.

Integrated functions include SiC-MOSFET's DESAT detection function, soft turn-off function at DESAT detection, DESAT detection FLT signal output function, gate bias voltage reduction detection/gate state monitoring RDY signal output function, and mirror clamp function.

This evaluation board is intended to be used with BM60052FV-C to drive the full-SiC power module for evaluation. However, it is not designed for mass-production use.

1-2. Schematic of the board

[BM60052FV-EVK-001]



Reference: [Full-SiC Power Module BSM300D12P2E001]: To be purchased separately

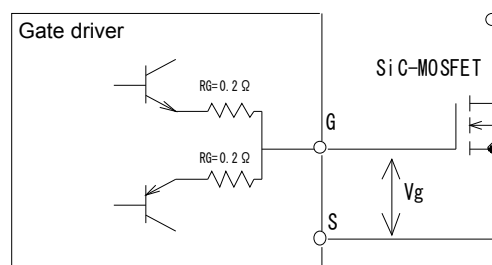


2-1. Performance specifications ($T_a=25^{\circ}\text{C}$. These are typical values and do not guarantee the characteristics of the evaluation board.)

Characteristic item	Standard/Rating	Remarks
Power voltage	12 VDC ~ 28 VDC (15 V typ., 24 V typ.) between Pin1 and Pin2	
Power current	0.8 A (power voltage 15 VDC) 0.5 A (power voltage 24 VDC)	* 1
Number of drive circuits	2	
Range of input signal frequency	DC ~ 100 kHz	
Minimum input ON pulse width	1.0 μs	* 6
Minimum input OFF pulse width	1.0 μs	
Input signal	5V 0-P	
Maximum gate drive charge	1500 nC	* 1, * 2
Output forward bias voltage (+Vg)	+17 V ~ +19 V	* 1
Output reverse bias voltage (-Vg)	-3 V ~ -5 V	* 1
Gate forward direction bias current (+I _g)	+7.5 A max ($P_{r w} \leq 0.5 \mu\text{s}$)	* 1, * 2
Gate drawing current (-I _g)	-8.5 A max ($P_{f w} \leq 0.5 \mu\text{s}$)	* 1, * 2
Rise response delay time (+T _{stg})	100 ns typ.	* 1, * 3
Fall response delay time (-T _{stg})	100 ns typ.	* 1, * 4
Rise time (T _r)	100 ns typ.	* 1, * 5
Fall time (T _f)	100 ns typ.	* 1, * 5
Withstand voltage	For one minute at AC 2500 V (between input and output)	
Repeatedly peak voltage	1200V voltage between TH7 and TH8, voltage between TH8 and TH8	
Insulation resistance	100 m Ω or more at DC 500 V (between input and output)	
DESAT detection voltage	4.0 V (min)	
Operating temperature range	-40 ~ +70°C	
Storage temperature range	-40 ~ +80°C	
Operating humidity range	30% to 90% RH (No dew-condensation)	

* 1 V_{in} : 15 V, 24 V; Load: Dummy load equivalent to BSM300D12P2E001, i.e., 1.6 Ω + 0.083 μf ; f : 100 kHz and Duty cycle: 50%

* 2 A gate resistance (R_G) of 0.2 Ω is inserted in the circuit for SiC-MOSFET gate driver as shown in the following figure.

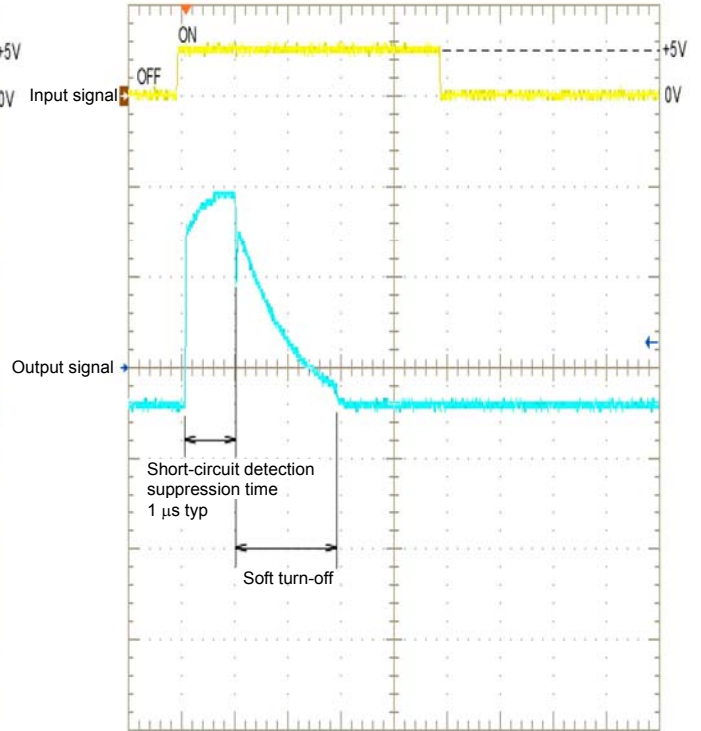
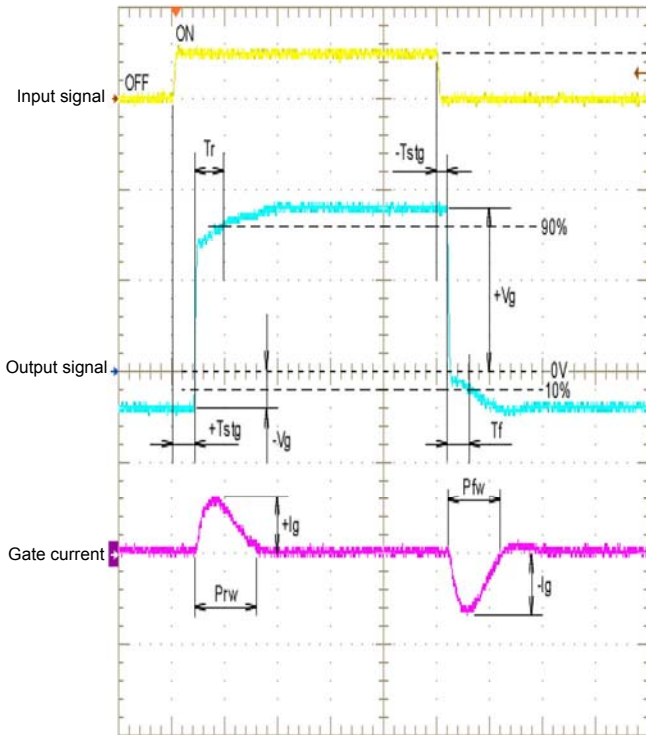


- * 3 +Tstg: The time from the rise of input signals until reaching 10% of the output gate signal peak value.
- * 4 -Tstg: The time from the fall of input signals until reaching 90% of the output gate signal peak value.
- * 5 Tr, Tf: The time taken for the transition between 10% and 90% of the output gate signal peak value.
- * 6 About 1 μs is defined for DESAT detection suppression after the gate rise.

2-2. Definition of output parameters

(1) At steady output

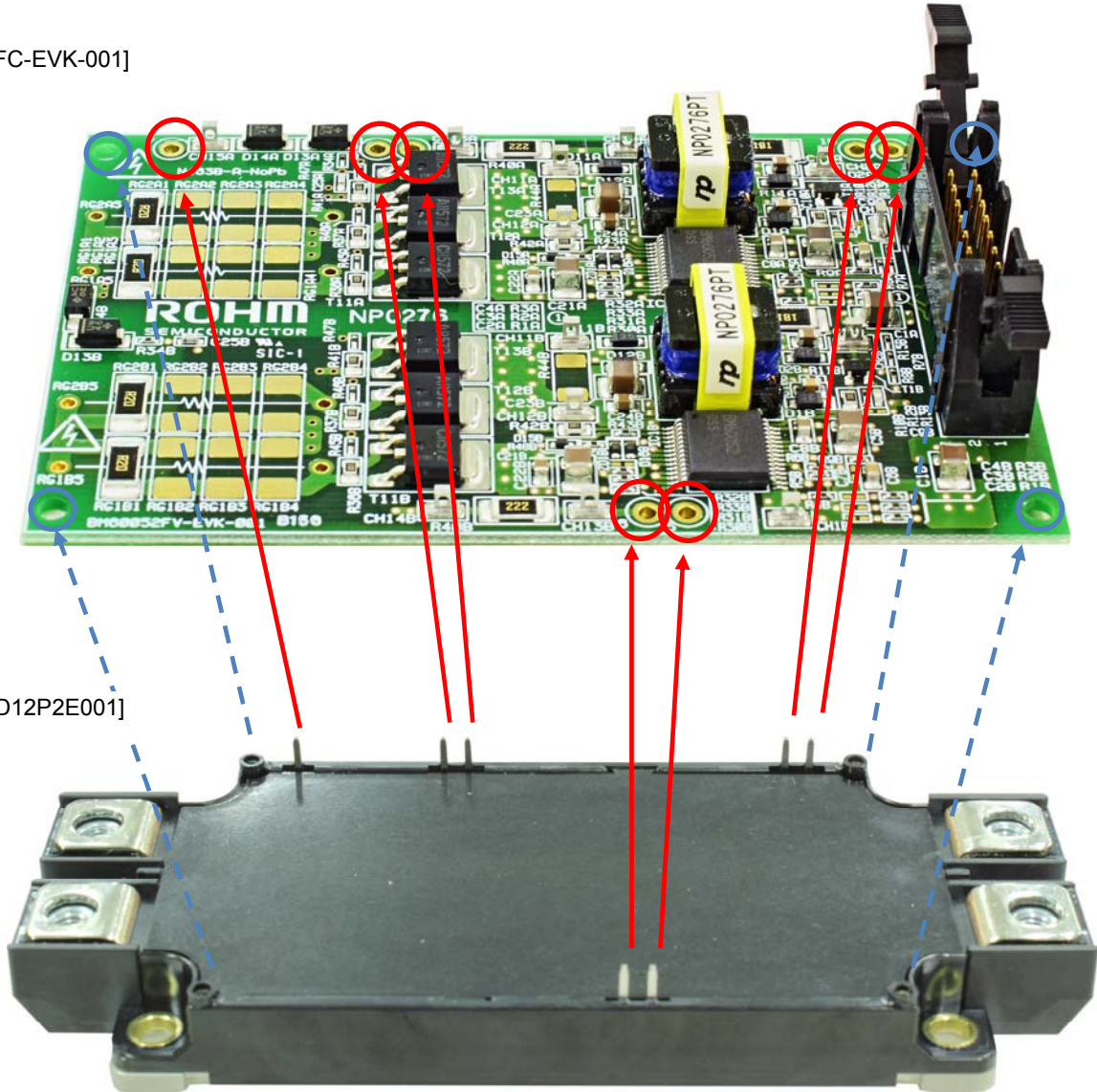
(2) At DESAT detection



3. Operating procedures

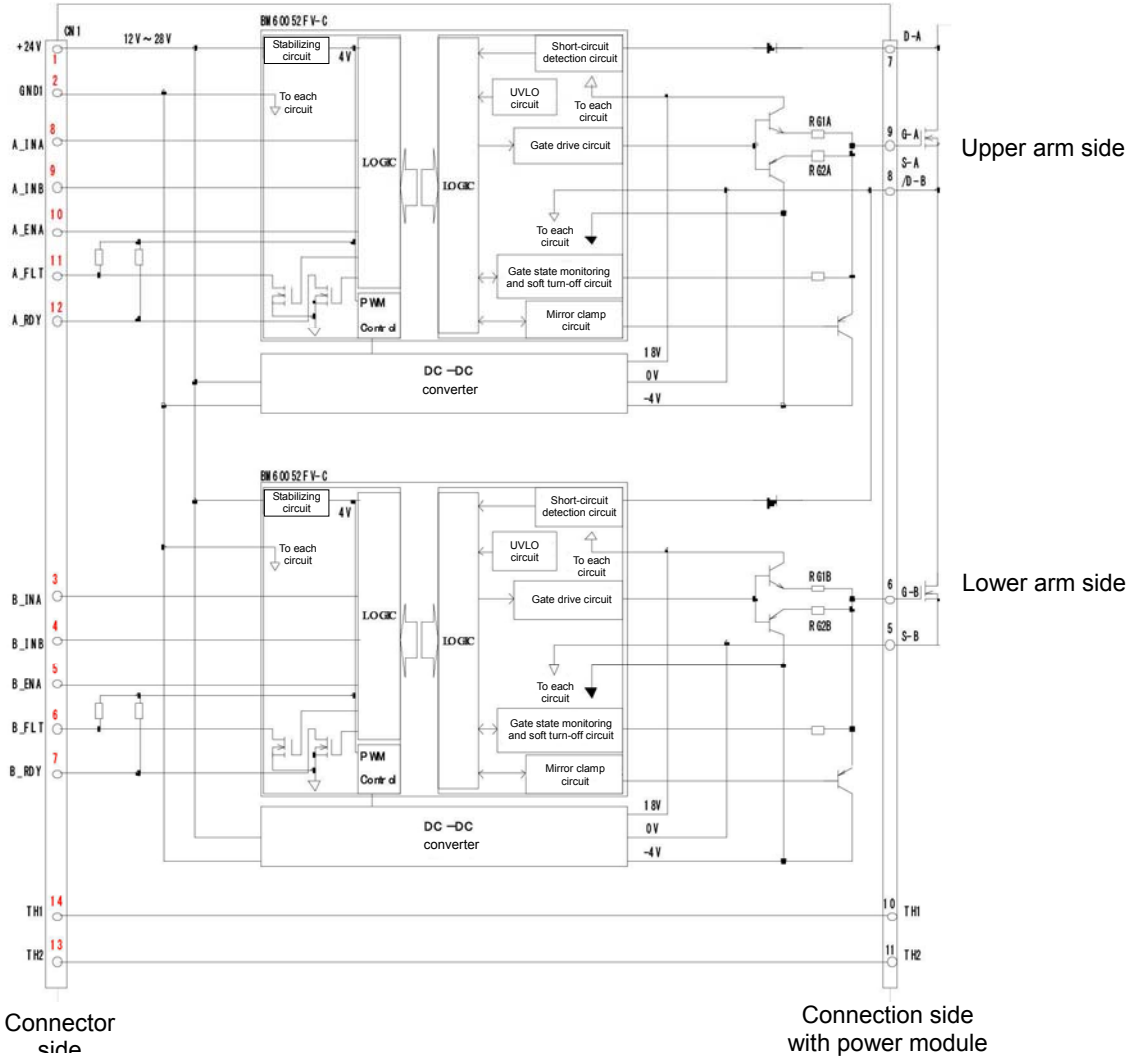
- (1) Place BM60052FV-EVK-001 on the full-SiC power module and make sure that the seven pins are correctly located. (See the red solid lines in the following figure)
- (2) Fix BM60052FV-EVK-001 using self-tap screws. (See the blue dotted lines in the following figure)
- (3) Solder the seven pins for electrical connection.

[BM60052FC-EVK-001]

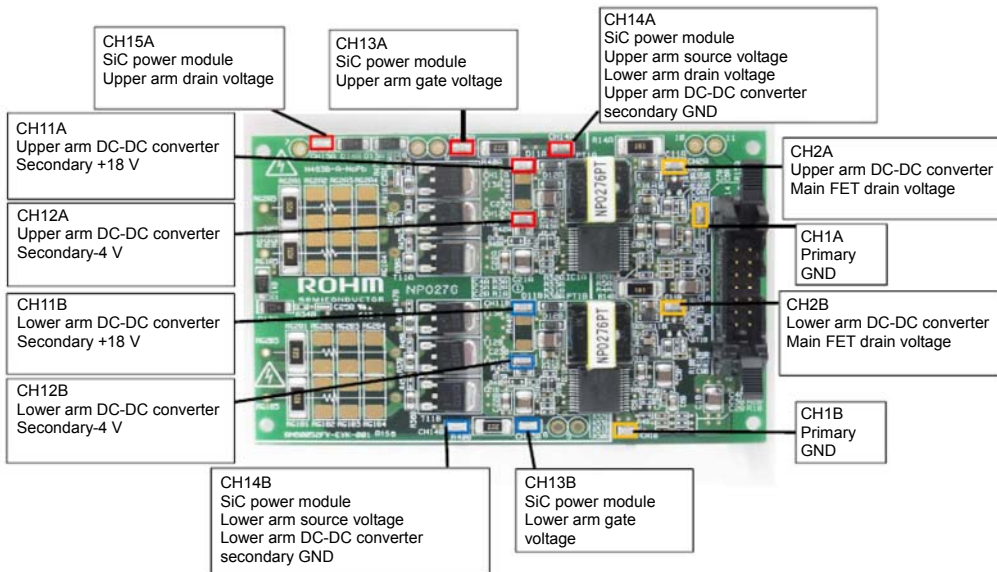


[BSM300D12P2E001]

4-1. Block diagram (check pin configuration)

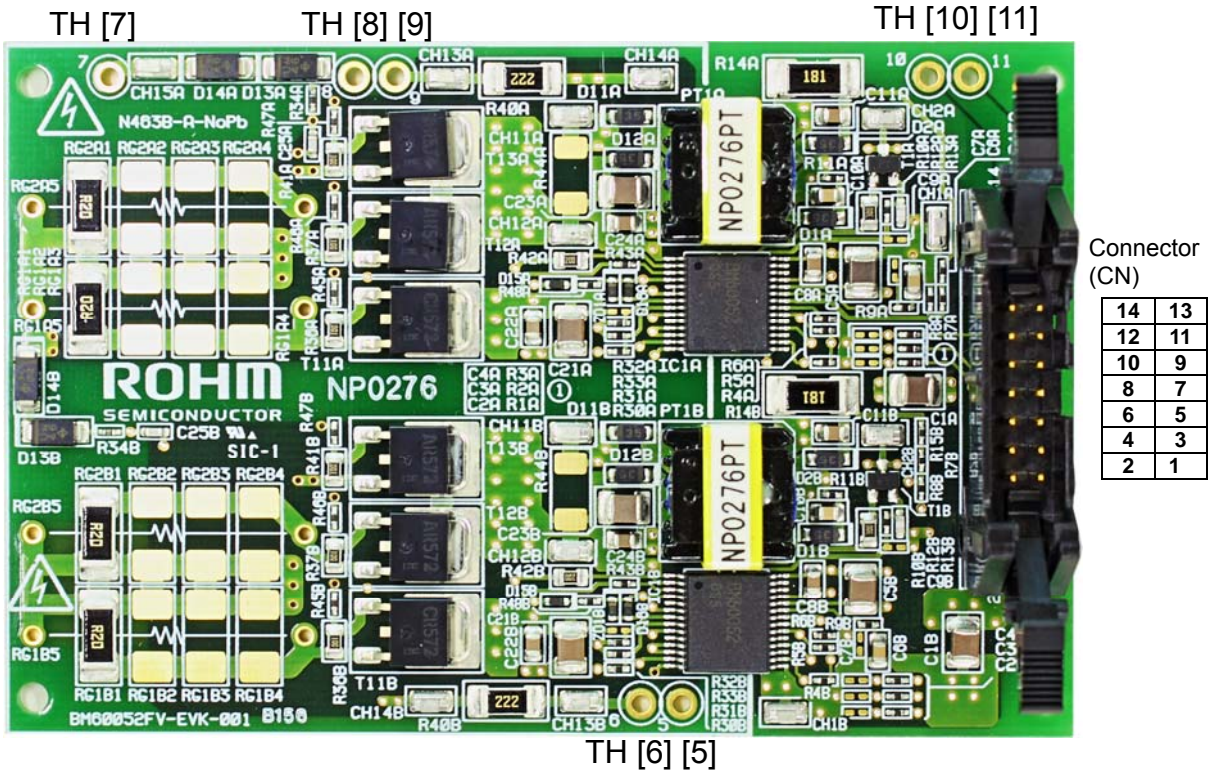


4-2. Description of check pins



* Yellow: Primary, Red: Secondary upper arm side, Blue: Secondary lower arm side
 The oscilloscope power supply should be floating. When measuring circuits with different GND potentials simultaneously, use a differential probe or other device to prevent ground fault or short circuit in the oscilloscope's GND terminal.

5-1. Through-hole pin layout, connector layout



5-2. Names of input/output terminals

Power supply, signal input/output:
 HIF3BA-14PA-2.54DSA (71) (Hirose Electric)
 (Connector side: CN 1-14)

Gate source output, drain input: $\phi 2.0$ mm through hole
 (Connection side with power module: upper figure [5] to [11])

CN	Signal name	Description
1	VDD	Input power (+12 V ~+28 V)
2	GND	Input power (GND)
3	B_INA	B ch input signal A
4	B_INB	B ch input signal B
5	B_ENA	B ch enable signal
6	B_FLT	B ch short circuit detection output
7	B_RDY	B ch UVLO, gate state monitoring output
8	A_INA	A ch input signal A
9	A_INB	A ch input signal B
10	A_ENA	A ch enable signal
11	A_FLT	A ch short-circuit detection output
12	A_RDY	A ch UVLO, gate state monitoring output
13	TH2	Thermistor terminal 11 (not used)
14	TH1	Thermistor terminal 10 (not used)

TH	Signal name	Description
5	S-B	B ch source output
6	G-B	B ch gate output
7	D-A	A ch drain input
8	S-A /D-B	A ch source output and B ch drain input
9	G-A	A ch gate output
10	TH1	Thermistor terminal 10 (not used)
11	TH2	Thermistor terminal 11 (not used)

X_A: Element-related terminal for upper arm

X_B: Element-related terminal for lower arm

For the thermistor terminals, TH1 and TH2 are only connected to each other on the substrate, and not to the IC.

A_XXX: A ch-related upper arm control-associated terminal
 B_XXX: B ch-related lower arm control-associated terminal

5-3. Fitting connectors

	Hirose Electric	Omron
Flat cable pressure welding-type connector	HIF3BA-14D-2.54R	XG4M-1430-T
Loose-wire crimp-type connector	HIF3BA-14D-2.54C	XG5N-141
Contact for loose wires	HIF3-2226SC(AWG22~AWG26)	XG5W-0231(AWG22~26)
	HIF3-2428SC(AWG24~AWG28)	XG5W-0232(AWG24~28)

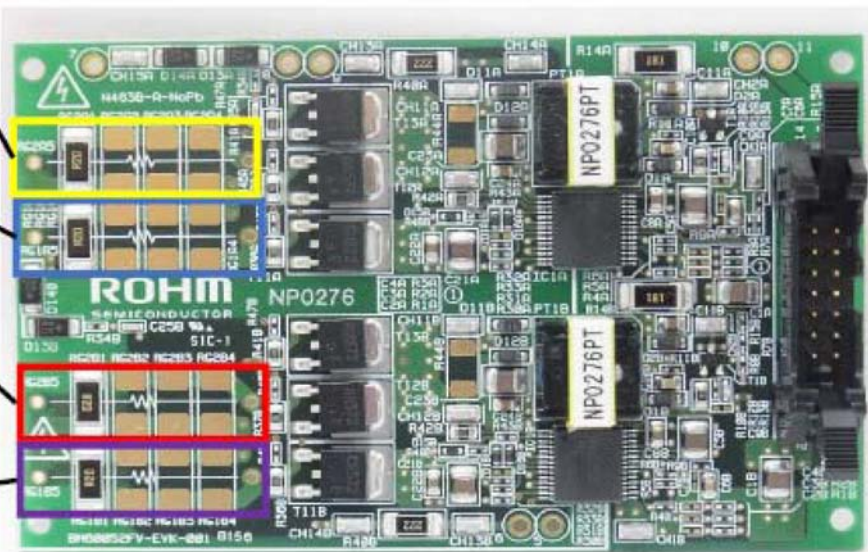
Note: For details, refer to the manufacturer's catalog.

6. Selection of gate resistance

The gate resistance of this product is 0.2 Ω, which is a standard level for BSM300D12P2E001. This can be changed to an optimum value according to your equipment. Make the required adjustment by paying attention to the operation and heat generation in each part.

Upper/lower arms		Circuit symbol	Substrate pattern layout/Implementation status
Upper arm side	Rise 5-parallel connection	RG1A1	Square shape chip resistor MCR100 (1 W_0.2 ΩJ, ROHM): Implemented
		RG1A2	Square shape chip resistor MCR100 (1 W, ROHM): Not implemented
		RG1A3	
		RG1A4	
		RG1A5	Through-hole diameter φ 1.2 mm and pitch 25.4 mm: Not implemented
	Fall 5-parallel connection	RG2A1	Square shape chip resistor MCR100 (1 W_0.2 ΩJ, ROHM): Implemented
		RG2A2	Square shape chip resistor MCR100 (1 W, ROHM): Not implemented
		RG2A3	
		RG2A4	
		RG2A5	Through-hole diameter φ 1.2 mm and pitch 25.4 mm: Not implemented
Lower arm side	Rise 5-parallel connection	RG1B1	Square shape chip resistor MCR100 (1 W_0.2 ΩJ, ROHM): Implemented
		RG1B2	Square shape chip resistor MCR100 (1 W, ROHM): Not implemented
		RG1B3	
		RG1B4	
		RG1B5	Through-hole diameter φ 1.2 mm and pitch 25.4mm: Not implemented
	Fall 5-parallel connection	RG2B1	Square shape chip resistor MCR100 (1 W_0.2 ΩJ, ROHM): Implemented
		RG2B2	Square shape chip resistor MCR100 (1 W, ROHM): Not implemented
		RG2B3	
		RG2B4	
		RG2B5	Through-hole diameter φ 1.2 mm and pitch 25.4 mm: Not implemented

- RG2A1 ~ RG2A5
Upper arm fall side
5-parallel connection
- RG1A1 ~ RG1A5
Upper arm rise side
5-parallel connection
- RG2B1 ~ RG2B5
Upper arm fall side
5-parallel connection
- RG1B1 ~ RG1B5
Lower arm rise side
5-parallel connection



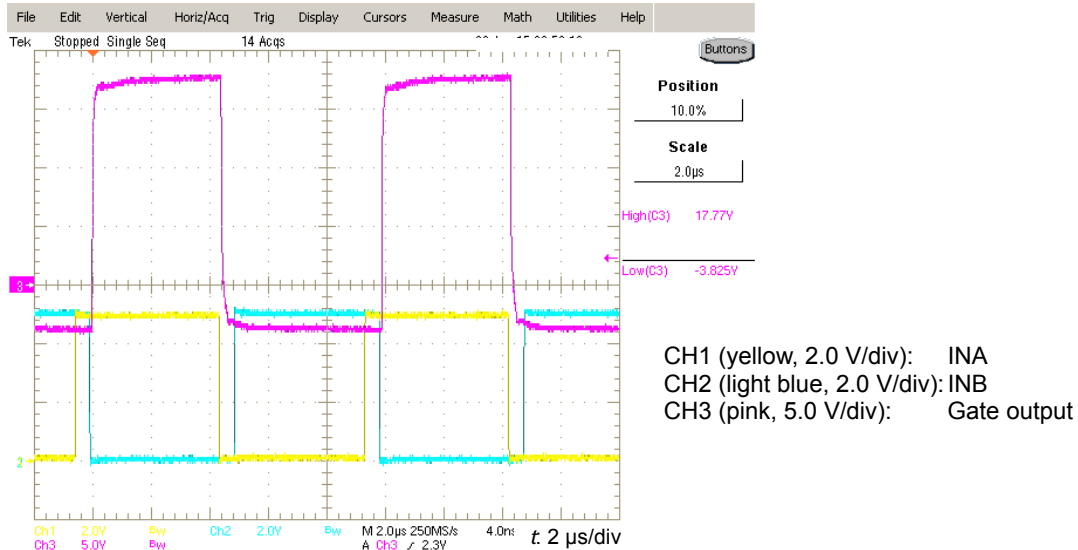
- The recommended minimum gate resistance value is 0.2 Ω.
- Increasing the gate resistance value will increase switching loss of the SiC power module, which may adversely affect the expected performance. Thus, a gate resistance as small as possible should be chosen.

7. Description of each function

■ Input signal and enable signal, determine the output logic.

CN10: A_ENA CN5: B_ENA	CN9: A_INB CN4: B_INB	CN8: A_INA CN3: B_INA	TH[9]: G-A (gate output) TH[6]: G-B (gate output)
L	x	x	L
H	H	x	L
H	L	L	L
H	L	H	H

Logic H and L level input voltages are in the range 2.0 V ~ 5.5 V and 0 ~ 0.8 V, respectively.



■ DESAT detection, FLT signal output (A_FLT, B_FLT)

When the gate output is high and SiC-MOSFET's V_{ds} is 4V or more, the gate voltage is lowered (soft turn-off) and FLT signals (8-pin) are output. (0 V at detection and 4 V at steady state).

This operation is cleared at the rise of input signal ENA.

The FLT terminal is pulled up with the VREG terminal on the evaluation substrate at 10 kΩ.

- A detection suppression time of about 1 μs is defined after the gate rise.
- For details of the DESAT detection function, refer to the data sheet of BM60052FV-C.

■ Gate bias voltage reduction detection (UVLO), gate state monitoring, RDY signal output (A_RDY, B_RDY)

When the gate bias voltage approximate 18V is decreased to approximate 14V because of abnormalities such as gate output short-circuit and an output over current, or the gate state monitoring finds an inconsistency between the input and output, a RDY signal will be output (0 V at detection and 4 V at steady state).

When the power voltage increases to the voltage reduction detection level, the operation returns to the steady state.

The RDY terminal is pulled up with the VREG terminal on the evaluation substrate at 10 kΩ.

- Gate state monitoring filter time: 1.5 μs ~ 2.5 μs

■ Mirror clamp function

While the gate output is low, when the OUT2 terminal falls below a certain voltage level, the mirror clamp function starts operating. Also, it starts operating at DESAT detection.

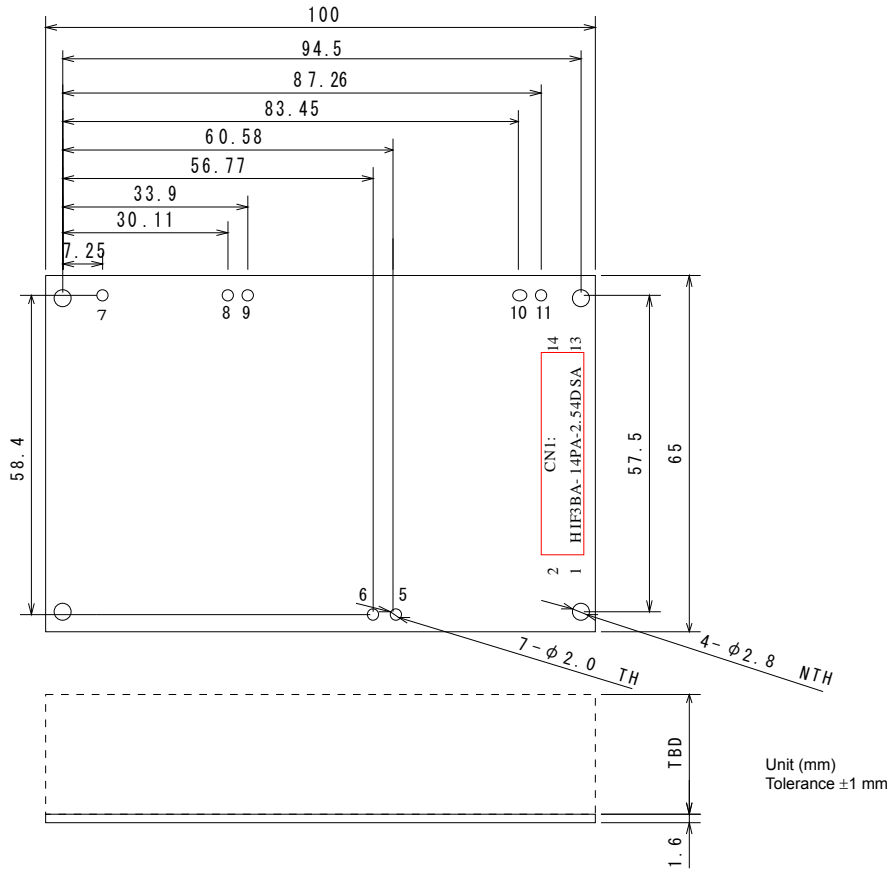
- Mirror clamp detection voltage: 1.8 V ~ 2.2 V (between G and S)
- For details of the mirror clamp function, refer to the data sheet of BM60052FV-C.

■ Thermal protection function

BM60052FV-C has temperature sensor voltage input terminals and integrates the thermal protection function. However, these are set up as unavailable for this evaluation board.

(The connection hole of the module is connected to the connector and not to BM60052FV-C.)

7. Outline drawing



■<High Voltage Safety Precautions>

◇ Read all safety precautions before use

Please note that this document covers only the BM60052FV-C evaluation board (BM60052FV-EVK-001) and its functions.
For additional information, please refer to the datasheet.

To ensure safe operation, please carefully read all precautions before handling the evaluation board



Depending on the configuration of the board and voltages used,

Potentially lethal voltages may be generated.

Therefore, please make sure to read and observe all safety precautions described in the red box below.

Before Use

- [1] Verify that the parts/components are not damaged or missing (i.e. due to the drops).
- [2] Check that there are no conductive foreign objects on the board.
- [3] Be careful when performing soldering on the module and/or evaluation board to ensure that solder splash does not occur.
- [4] Check that there is no condensation or water droplets on the circuit board.

During Use

- [5] Be careful to not allow conductive objects to come into contact with the board.
- [6] **Brief accidental contact or even bringing your hand close to the board may result in discharge and lead to severe injury or death.**
Therefore, DO NOT touch the board with your bare hands or bring them too close to the board.
In addition, as mentioned above please exercise extreme caution when using conductive tools such as tweezers and screwdrivers.
- [7] Please proceed carefully, taking note of any condensation when operating at low temperatures or discoloration/leakage of the parts/board due to excessive heat.
- [8] Be sure to wear insulated gloves when handling is required during operation.

After Use

- [9] Even after the power has been turned off, please note that burns can still occur due to contact with superheated parts or electric shock caused by charge stored in the capacitor.
- [10] Protect against electric shocks by wearing insulated gloves when handling.

This evaluation board is intended for use only in research and development facilities and should be handled **only by qualified personnel familiar with all safety and operating procedures.**

We recommend carrying out operation in a safe environment that includes the use of high voltage signage at all entrances, safety interlocks, and protective glasses.

Notes

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